REMARKS

The examiner has rejected claims 1-13 under 35 U.S.C. 103 as unpatentable over art discussed in the background section of the application in view of Bothelo, U.S. patent 5,477,544.

Claim Amendments

Claims 1-4 and 7-10 have been cancelled without prejudice.

Claim 5-6 have been made dependent upon new claim 13 instead of cancelled claim 4.

A limitation regarding board identification information has been added to claim 11.

Claim 12 has been made dependent on the intended claim 11, instead of claim 10 that lacked proper antecedent basis for element of claim 12.

New Claim 13 is of scope roughly equivalent to the scope of former claim 4, including claim 4's antecedent claims. New dependent claim 14 adds a limitation having basis in paragraph 42 of the application, regarding selecting a configuration code compatible with a particular board based upon a board identification that is read through the common connection point

Claims 13 and 14

As cited by the Examiner, the apparatus of Bothelo, U.S. patent 5477544, is a device for selectively coupling a test port of test apparatus (Bothelo 14) successively to test ports of multiple test ports of multiple devices-under-test (DUTs Bothelo 16).

As the Examiner noticed, Bothelo does not provide an element of reading a board identification over the serial bus, or of verifying compatibility of the configuration code with the read board identification. In rejecting claim 4, the Examiner relied on Paragraph 13 of Applicant's background to provide this element.

Applicant fails to see any mention of reading board identification information in paragraph 13, or in any paragraph adjacent to paragraph 13, of the specification. Applicant is, however, aware of the existence of serial identification EEPROMS on many standard DIMM (dual-inline memory module) devices, where a system using DIMMs can read timing parameters from the serial identification EEPROMS.

Applicant stated in paragraph 13 of the background that the configuration system must have knowledge of the "JTAG bus configuration of the board". The configuration information of prior art devices typically is required in advance of connecting a tester to the board, and required information includes the number and interface type of EEPROM devices on the particular JTAG bus.

The nearest thing to a reference to a board identification Applicant sees in a paragraph near paragraph 13 is a reference to the fact that many programmable devices, including FPGA devices, perform a checksum verification of code as these devices load code from an EEPROM.

Checksum verification of this type is compatibility verification *at programmed system run time* of code in an EEPROM with a particular FPGA. This is not compatibility verification with the board *at EEPROM programming time* as disclosed in the detailed description and as claimed in former claim 4 and new claim 13. At this point it is too late to identify different, correct, code since the programming system may no longer be accessible. Even were code acceptable to the FPGA device with correct checksum, that code may program the FPGA to perform functions totally inappropriate for the circuit board, or inappropriate for the system containing the board.

There can be a wide variety of different boards having the same number and interface type of EEPROM devices on a particular JTAG bus of the board. For example, a first board implementing a controller may have a pair of EEPROM devices, with one EEPROM containing firmware for a microprocessor, and the second EEPROM containing an FPGA code and, in an otherwise unused location, a board identification. A second board implementing a network interface could have FPGA code in both EEPROMs and no microprocessor.

Different system boards, even different revisions of the same model, may require different FPGA code due to minor changes in component types both of the FPGA and of other devices on the boards. Having a machine-readable board identity and version code, and verifying it before programming EEPROMs on each board, ensures that programmable devices on that board are programmed with code intended for the system.

The fact that many elements in the claims are old does not necessarily make the invention obvious under 35 U.S.C. 103 absent a suggestion in the art that the elements be combined in a particular way. Otherwise virtually every mechanical device would be obvious because screws, rivets, pistons, piston rings, gears, valves, bolts, turbine blades, bearings, cams, and shafts as individual components are well known in the art.

In applicant's system as now claimed in Claims 11 and 13, board identification information is read from the board. As claimed in Claim 14, this board identification is used by the configuration system to select an appropriate configuration code from a file of configuration codes. Applicant's system therefore allows an attached configuration system to poll the circuit boards of the system to determine their type, and to then program EEPROMS of each circuit board with firmware, including FPGA code firmware, appropriate for those particular board types in that particular system. This combination Applicant believes is novel.

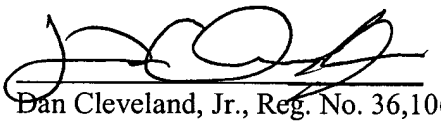
CONCLUSION

Applicant submits that the invention as described in the amended claims is not anticipated under 35 U.S.C. 102 or obvious under 35 U.S.C 103 under any combination of Applicant's admitted background with Bothello.

Applicant respectfully requests that the enclosed amendments be entered and the application reconsidered in light of the above remarks.

If, in the Examiner's opinion, prosecution of the present application may be expedited with a telephone conference, the Examiner is encouraged to contact Applicant's attorney at the number below.

Respectfully submitted,

By: 

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